ANALOG DEVICES

High Speed, Video Difference Amplifier

AD830

FEATURES

Differential Amplification
- **Wide Common-Mode Voltage Range: +12.8 V, –12 V**
- **Differential Voltage Range: ±2 V**
- **High CMRR: 60 dB @ 4 MHz**
- **Built-in Differential Clipping Level: ±2.3 V**

Fast Dynamic Performance
- **85 MHz Unity Gain Bandwidth**
- **35 ns Settling Time to 0.1%**
- **360 V/µs Slew Rate**

Symmetrical Dynamic Response

Excellent Video Specifications
- **Differential Gain Error: 0.06%**
- **Differential Phase Error: 0.08°**
- **15 MHz (0.1 dB) Bandwidth**

Flexible Operation
- **High Output Drive of ±50 mA min**
- **Specified with Both ±5 V and ±15 V Supplies**

Low Distortion: THD = –72 dB @ 4 MHz

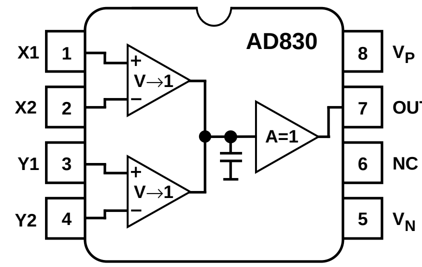
Excellent DC Performance: 3 mV max Input Offset Voltage

APPLICATIONS

Differential Line Receiver
High Speed Level Shifter
High Speed In-Amp
Differential to Single Ended Conversion
Resistorless Summation and Subtraction
High Speed A/D Driver

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

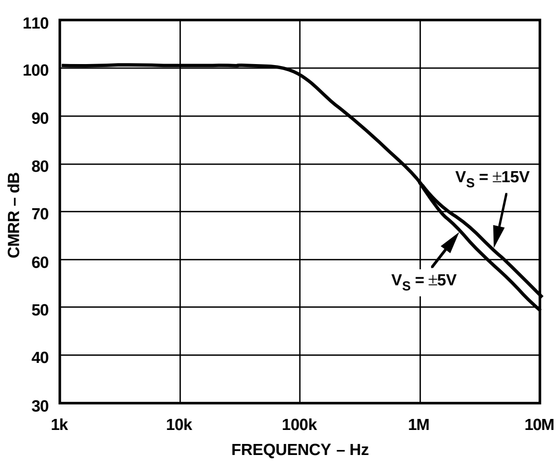


PRODUCT DESCRIPTION

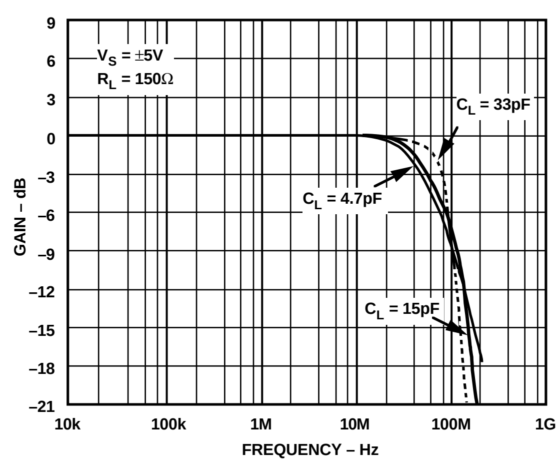
The AD830 is a wideband, differencing amplifier designed for use at video frequencies but also useful in many other applications. It accurately amplifies a fully differential signal at the input and produces an output voltage referred to a user-chosen level. The undesired common-mode signal is rejected, even at high frequencies. High impedance inputs ease interfacing to finite source impedances and thus preserve the excellent common-mode rejection. In many respects, it offers significant improvements over discrete difference amplifier approaches, in particular in high frequency common-mode rejection.

The wide common-mode and differential-voltage range of the AD830 make it particularly useful and flexible in level shifting applications, but at lower power dissipation than discrete solutions. Low distortion is preserved over the many possible differential and common-mode voltages at the input and output.

Good gain flatness and excellent differential gain of 0.06% and phase of 0.08° make the AD830 suitable for many video system applications. Furthermore, the AD830 is suited for general purpose signal processing from dc to 10 MHz.



Common-Mode Rejection Ratio vs. Frequency



Closed-Loop Gain vs. Frequency, Gain = +1

REV. A

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AD830–SPECIFICATIONS (V_S = ±15 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted)

Parameter	Conditions	AD830J/A Min	AD830J/A Typ	AD830J/A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Units
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = 1, V_{OUT} = 100 mV rms	75	85		75	85		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, V_{OUT} = 100 mV rms	11	15		11	15		MHz
Differential Gain Error	0 to +0.7 V, Frequency = 4.5 MHz		0.06	0.09		0.06	0.09	%
Differential Phase Error	0 to +0.7 V, Frequency = 4.5 MHz		0.08	0.12		0.08	0.12	Degrees
Slew Rate	2 V Step, R_L = 500 Ω		360			360		V/µs
	4 V Step, R_L = 500 Ω		350			350		V/µs
3 dB Large Signal Bandwidth	Gain = 1, V_{OUT} = 1 V rms	38	45		38	45		MHz
Settling Time, Gain = 1	V_{OUT} = 2 V Step, to 0.1%		25			25		ns
	V_{OUT} = 4 V Step, to 0.1%		35			35		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		–82			–82		dBc
	2 V p-p, Frequency = 4 MHz		–72			–72		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = 1		±1.5	±3		±1.5	±3	mV
	Gain = 1, T_{MIN}–T_{MAX}			±5			±7	mV
Open Loop Gain	DC	64	69		64	69		dB
Gain Error	R_L = 1 kΩ, G = ±1		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L= 1 kΩ,	–1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
Gain = 1	–1.5 V ≤ X ≤ +1.5 V		0.035	0.07		0.035	0.07	% FS
	–2 V ≤ X ≤ +2 V		0.15	0.4		0.15	0.4	% FS
Input Bias Current	V_{IN} = 0 V, +25°C to T_{MAX}		5	10		5	10	µA
	V_{IN} = 0 V, T_{MIN}		7	13		8	17	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN}–T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level[2]	Pins 1 and 2 Inputs Only	±2.1	±2.3		±2.1	±2.3		V
Common-Mode Voltage Range	V_{DM} = ±1 V	–12.0		+12.8	–12.0		+12.8	V
CMRR	DC, Pins 1, 2, ±10 V	90	100		90	100		dB
	DC, Pins 1, 2, ±10 V, T_{MIN}–T_{MAX}	88			86			dB
	Frequency = 4 MHz	55	60		55	60		dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 1 kΩ	±12	+13.8, –13.8		±12	+13.8, –13.8		V
	R_L ≥ 1 kΩ, ±16.5 V_S	±13	+15.3, –14.7		±13	+15.3, –14.7		V
Short Circuit Current	Short to Ground		±80			±80		mA
Output Current	R_L = 150 Ω	±50			±50			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN}–T_{MAX}		14.5	17		14.5	17	mA
+ PSRR (to V_P)	DC, G = 1		86			86		dB
– PSRR (to V_N)	DC, G = 1		68			68		dB
PSRR	DC, G = 1, ±5 to ±15 V_S	66	71		66	71		dB
PSRR	DC, G = 1, ±5 to ±15 V_S, T_{MIN}–T_{MAX}	62	68		60	68		dB

NOTES

[1]See Standard Military Drawing 5962-9313001MPA for specifications.

[2]Clipping level function on X channel only.

Specifications subject to change without notice.

(V_S = ±5 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted)

Parameter	Conditions	AD830J/A Min	AD830J/A Typ	AD830J/A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Units
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = 1, V_{OUT} = 100 mV rms	35	40		35	40		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, V_{OUT} = 100 mV rms	5	6.5		5	6.5		MHz
Differential Gain Error	0 to +0.7 V, Frequency = 4.5 MHz, G = +2		0.14	0.18		0.14	0.18	%
Differential Phase Error	0 to +0.7 V, Frequency = 4.5 MHz, G = +2		0.32	0.4		0.32	0.4	Degrees
Slew Rate, Gain = 1	2 V Step, R_L = 500 Ω		210			210		V/µs
	4 V Step, R_L = 500 Ω		240			240		V/µs
3 dB Large Signal Bandwidth	Gain = 1, V_{OUT} = 1 V rms	30	36		30	36		MHz
Settling Time	V_{OUT} = 2 V Step, to 0.1%		35			35		ns
	V_{OUT} = 4 V Step, to 0.1%		48			48		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		–69			–69		dBc
	2 V p-p, Frequency = 4 MHz		–56			–56		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		$nV/\sqrt{Hz}$
Input Current Noise			1.4			1.4		$pA/\sqrt{Hz}$
DC PERFORMANCE								
Offset Voltage	Gain = 1		±1.5	±3		±1.5	±3	mV
	Gain = 1, T_{MIN}–T_{MAX}			±4			±5	mV
Open Loop Gain	DC	60	65		60	65		dB
Unity Gain Accuracy	R_L = 1 kΩ		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L= 1 kΩ	–1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
	–1.5 V ≤ X ≤ +1.5 V		0.045	0.07		0.045	0.07	% FS
	–2 V ≤ X ≤ +2 V		0.23	0.4		0.23	0.4	% FS
Input Bias Current	V_{IN} = 0 V, +25°C to T_{MAX}		5	10		5	10	µA
	V_{IN} = 0 V, T_{MIN}		7	13		8	17	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN}–T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level[2]	Pins 1 and 2 Inputs Only	±2.0	±2.2		±2.0	±2.2		V
Common-Mode Voltage Range	V_{DM} = ±1 V	–2.0		+2.9	–2.0		+2.9	V
CMRR	DC, Pins 1, 2, +4 V to –2 V	90	100		90	100		dB
	DC, Pins 1, 2, +4 V to –2 V, T_{MIN}–T_{MAX}	88			86			dB
	Frequency = 4 MHz	55	60		55	60		dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 150 Ω	±3.2	±3.5		±3.2	±3.5		V
	R_L ≥ 150 Ω, ±4 V_S	±2.2	+2.7, –2.4		±2.2	+2.7, –2.4		V
Short Circuit Current	Short to Ground		–55, +70			–55, +70		mA
Output Current		±40			±40			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN}–T_{MAX}		13.5	16		13.5	16	mA
+ PSRR (to V_P)	DC, G = 1, Offset		86			86		dB
– PSRR (to V_N)	DC, G = 1, Offset		68			68		dB
PSRR (Dual Supply)	DC, G = 1, ±5 to ±15 V_S	66	71		66	71		dB
PSRR (Dual Supply)	DC, G = 1, ±5 to ±15 V_S, T_{MIN}–T_{MAX}	62	68		60	68		dB

NOTES
[1]See Standard Military Drawing 5962-9313001MPA for specifications.
[2]Clipping level function on X channel only.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] . . . . Observe Derating Curves
Output Short Circuit Duration . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . $\pm V_S$
Differential Input Voltage . . . . $\pm V_S$
Storage Temperature Range (Q) . . . . –65°C to +150°C
Storage Temperature Range (N) . . . . –65°C to +125°C
Storage Temperature Range (R) . . . . –65°C to +125°C
Operating Temperature Range
  AD830J . . . . 0°C to +70°C
  AD830A . . . . –40°C to +85°C
  AD830S . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD830 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the AD830 in the "overheated" condition for an extended period can result in permanent damage to the device. To ensure proper operation, it is important to observe the recommended derating curves.

While the AD830 output is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. If the output is shorted to a supply rail for an extended period, then the amplifier may be permanently destroyed.

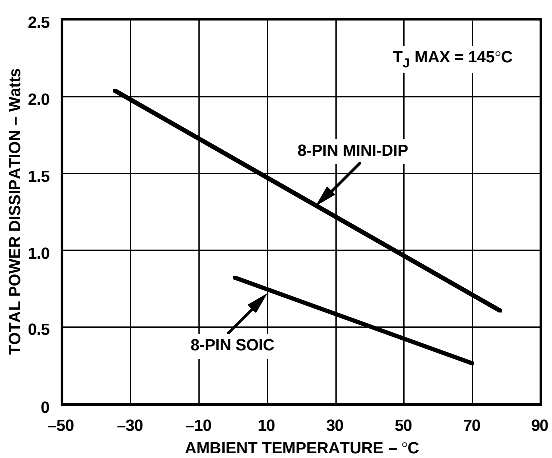
ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD830 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

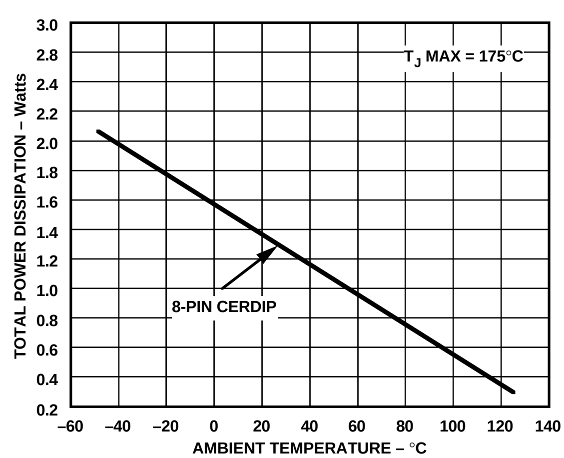
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD830AN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD830JR	0°C to +70°C	8-Pin SOIC	R-8
5962-9313001MPA*	–55°C to +125°C	8-Pin Cerdip	Q-8

*See Standard Military Drawing for specifications.



Maximum Power Dissipation vs. Temperature, Mini-DIP and SOIC Packages



Maximum Power Dissipation vs. Temperature, Cerdip Package

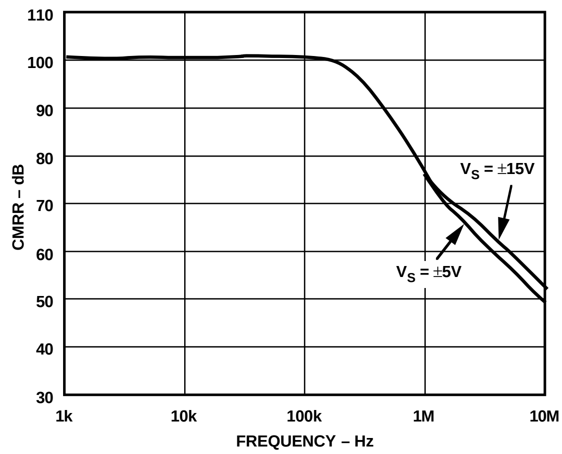


Figure 1. Common-Mode Rejection Ratio vs. Frequency

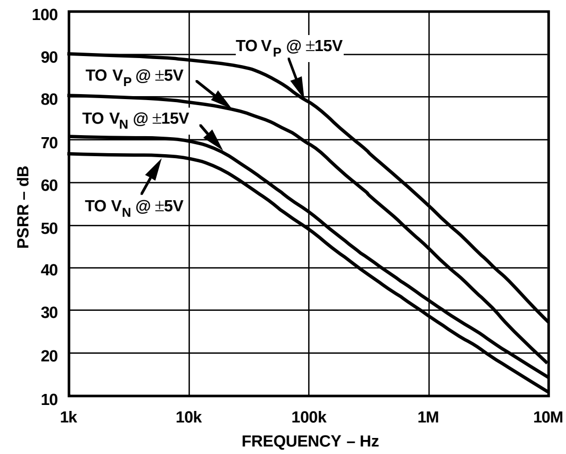


Figure 4. Power Supply Rejection Ratio vs. Frequency

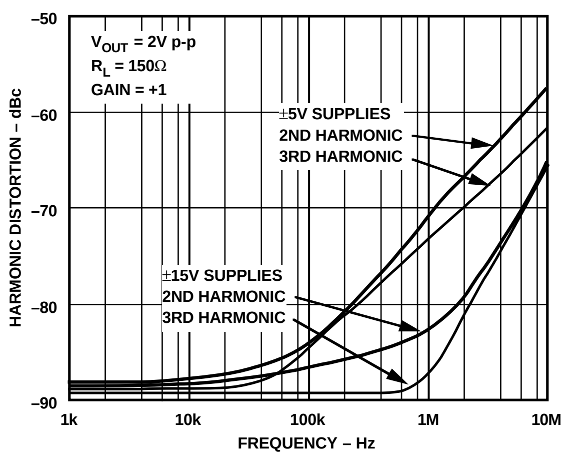


Figure 2. Harmonic Distortion vs. Frequency

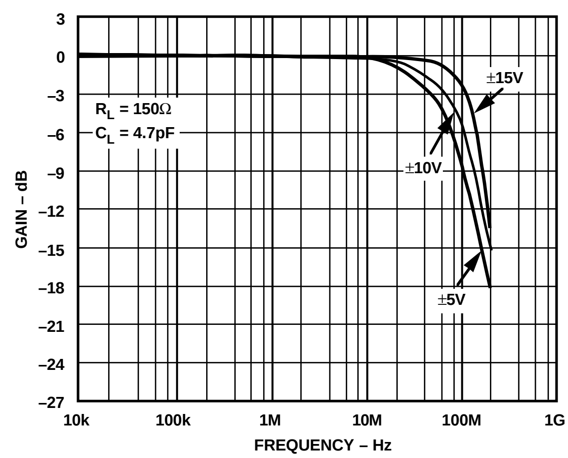


Figure 5. Closed-Loop Gain vs. Frequency G = +1

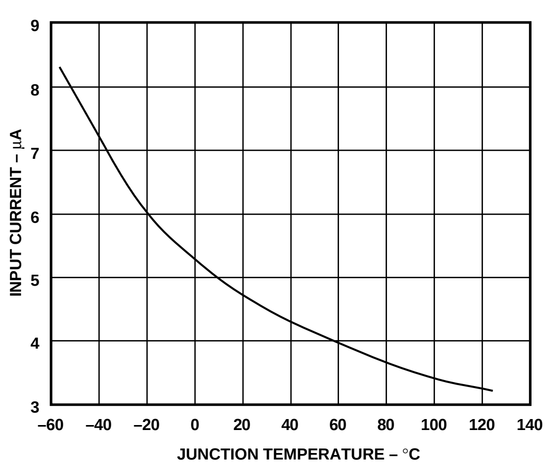


Figure 3. Input Bias Current vs. Temperature

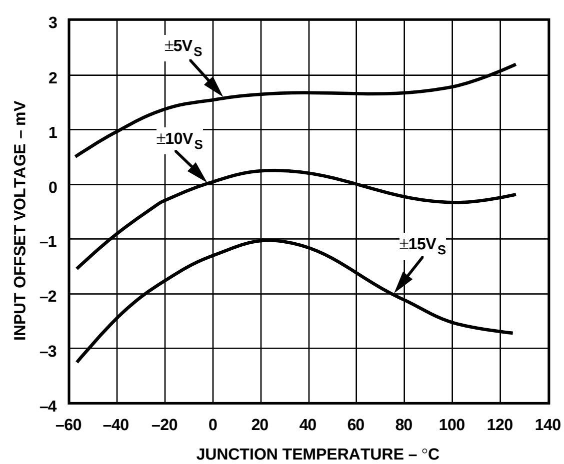


Figure 6. Input Offset Voltage vs. Temperature

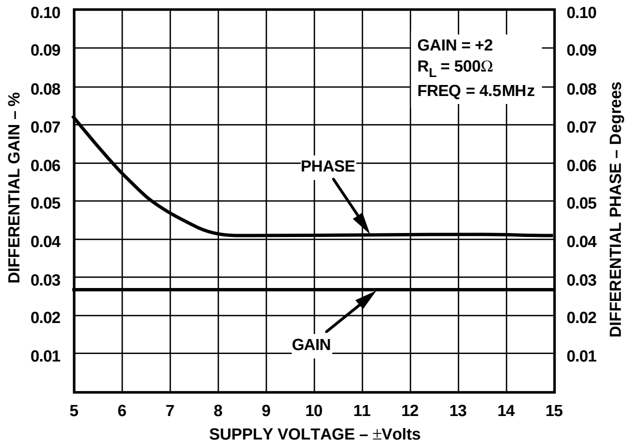


Figure 7. Differential Gain and Phase vs. Supply Voltage, R_L = 500 Ω

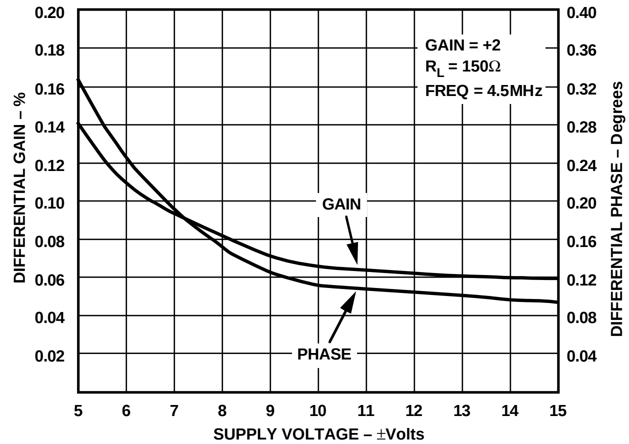


Figure 10. Differential Gain and Phase vs. Supply Voltage, R_L = 150 Ω

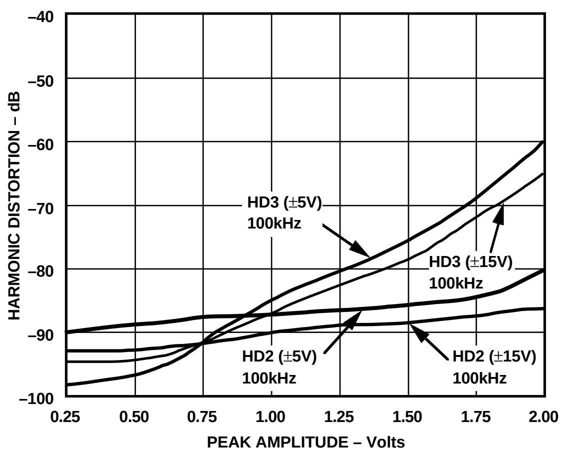


Figure 8. Harmonic Distortion vs. Peak Amplitude, Frequency = 100 kHz

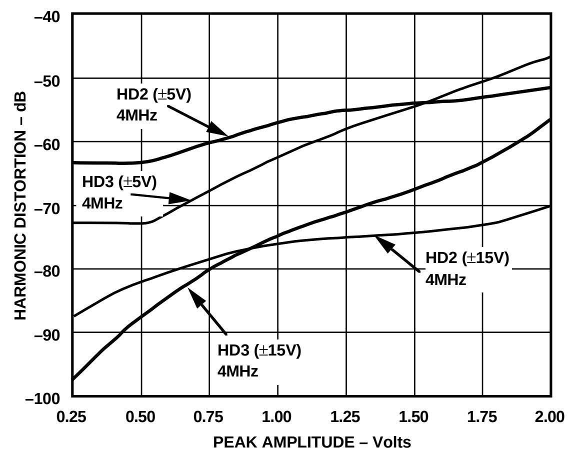


Figure 11. Harmonic Distortion vs. Peak Amplitude, Frequency = 4 MHz

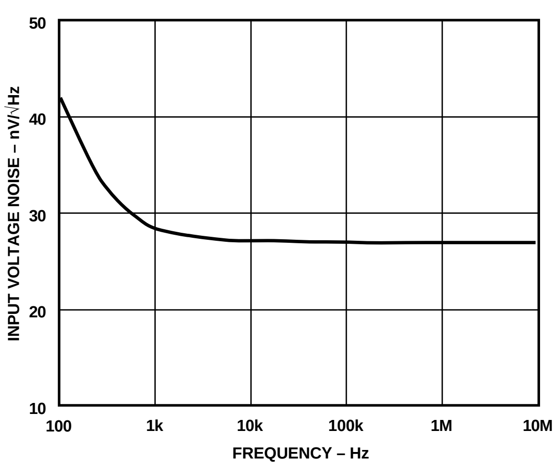


Figure 9. Noise Spectral Density

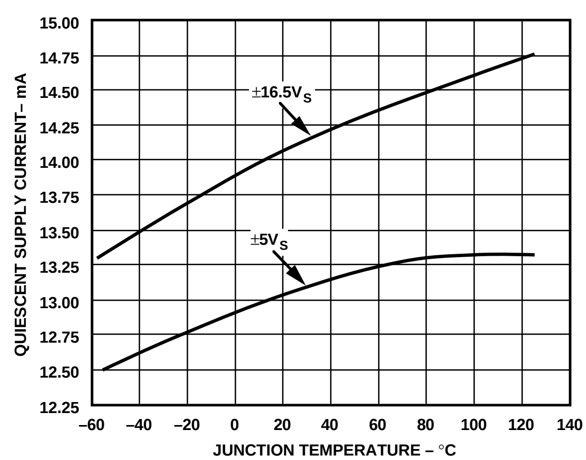


Figure 12. Supply Current vs. Junction Temperature

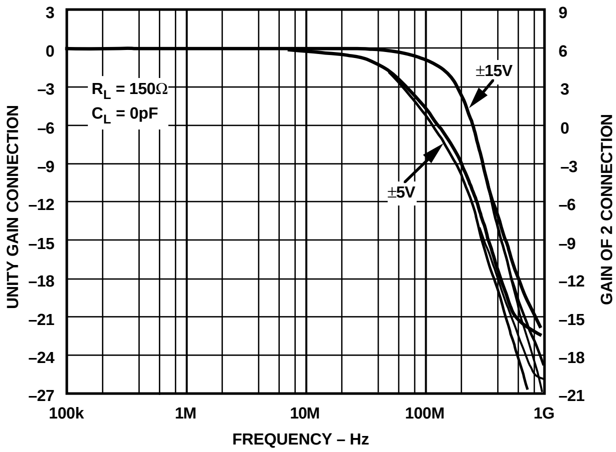


Figure 13. Closed-Loop Gain vs. Frequency for the Three Common Connections of Figure 16

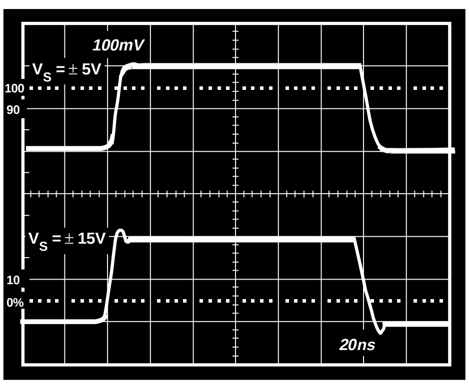


Figure 14. Small Signal Pulse Response, R_L = 150 Ω, C_L = 4.7 pF, G = +1

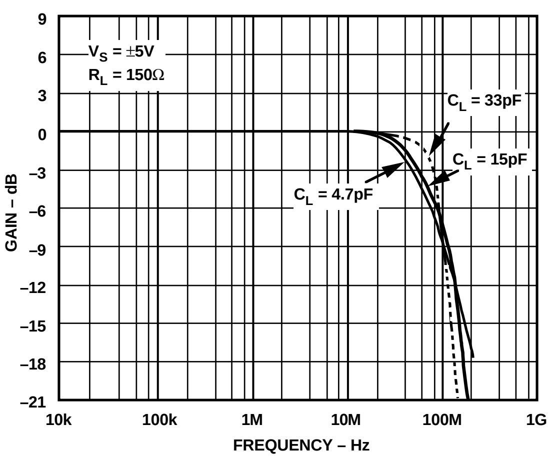


Figure 15. Closed-Loop Gain vs. Frequency vs. C_L, G = +1. V_S = ±5 V

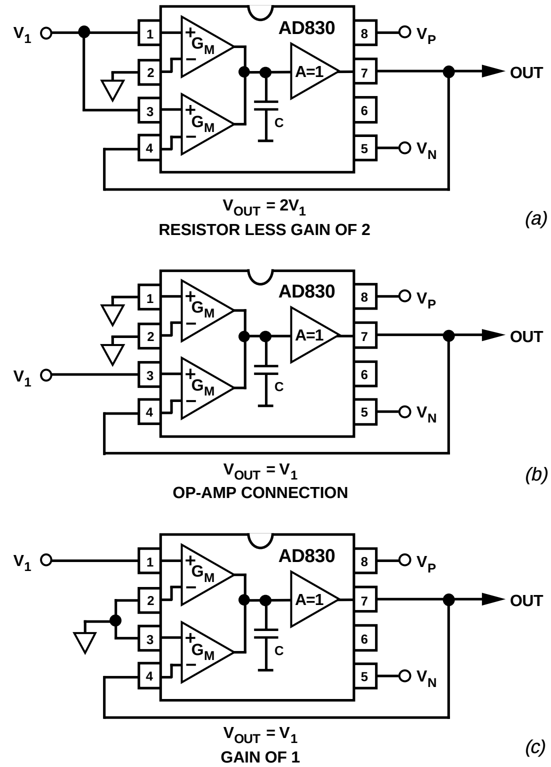


Figure 16. Connection Diagrams

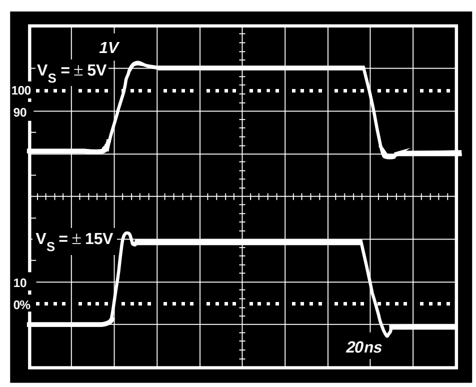


Figure 17. Large Signal Pulse Response, R_L = 150 Ω, C_L = 4.7 pF, G = +1

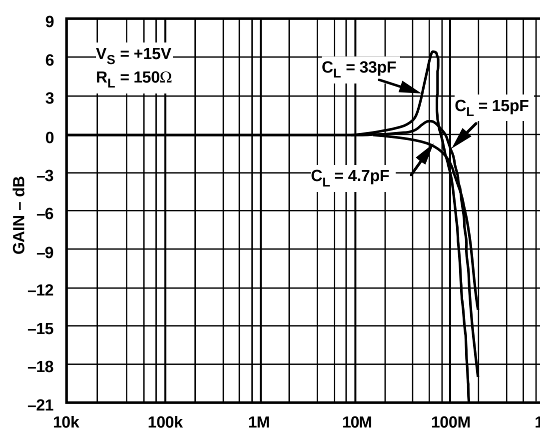


Figure 18. Closed-Loop Gain vs. Frequency, vs. C_L, G = +1. V_S = ±15 V

TRADITIONAL DIFFERENTIAL AMPLIFICATION

In the past, when differential amplification was needed to reject common-mode signals superimposed with a desired signal; most often the solution used was the classic op amp based difference amplifier shown in Figure 19. The basic function $V_O = V_1 – V_2$ is simply achieved, but the overall performance is poor and the circuit possesses many serious problems that make it difficult to realize a robust design with moderate to high levels of performance.

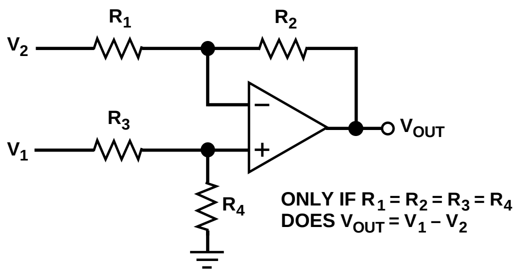


Figure 19. Op Amp Based Difference Amplifier

PROBLEMS WITH THE OP AMP BASED APPROACH

- Low Common-Mode Rejection Ratio (CMRR)
- Low Impedance Inputs
- CMRR Highly Sensitive to the Value of Source R
- Different Input Impedance for the + and – Input
- Poor High Frequency CMRR
- Requires Very Highly Matched Resistors R_1–R_4 to Achieve High CMRR
- Halves the Bandwidth of the Op Amp
- High Power Dissipation in the Resistors for Large Common-Mode Voltage

AD830 FOR DIFFERENTIAL AMPLIFICATION

The AD830 amplifier was specifically developed to solve the listed problems with the discrete difference amplifier approach. Its topology, discussed in detail in a later section, by design acts as a difference amplifier. The circuit of Figure 20 shows how simply the AD830 is configured to produce the difference of two signals V_1 and V_2, in which the applied differential signal is exactly reproduced at the output relative to a separate output common. Any common-mode voltage present at the input is removed by the AD830.

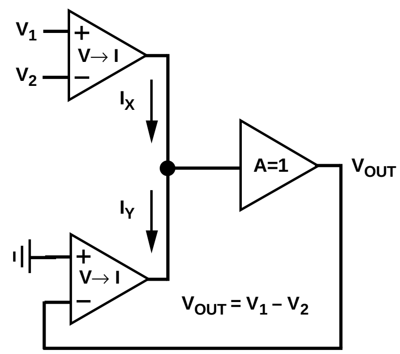


Figure 20. AD830 as a Difference Amplifier

ADVANTAGEOUS PROPERTIES OF THE AD830

- High Common-Mode Rejection Ratio (CMRR)
- High Impedance Inputs
- Symmetrical Dynamic Response for +1 and –1 Gain
- Low Sensitivity to the Value of Source R
- Equal Input Impedance for the + and – Input
- Excellent High Frequency CMRR
- No Halving of the Bandwidth
- Constant Power Distortion vs. Common-Mode Voltage
- Highly Matched Resistors Not Needed

UNDERSTANDING THE AD830 TOPOLOGY

The AD830 represents Analog Devices' first amplifier product to embody a powerful alternative amplifier topology. Referred to as active feedback, the topology used in the AD830 provides inherent advantages in the handling of differential signals, differing system commons, level shifting and low distortion, high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits or is superior to op amp based equivalent circuits. With this in mind, it is important to understand the internal structure of the AD830.

The topology, reduced to its elemental form, is shown below in Figure 21. Nonideal effects such as nonlinearity, bias currents and limited full scale are omitted from this model for simplicity, but are discussed later. The key feature of this topology is the use of two, identical voltage-to-current converters, G_M, that make up input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage to current converters possess fully differential inputs, high linearity, high input impedance and wide voltage range operation. This enables the part to handle large amplitude differential signals; they also provide high common-mode rejection, low distortion and negligible loading on the source. The label, G_M, is meant to convey that the transconductance is a large signal quantity, unlike in the front-end of most op amps. The two G_M stage current outputs I_X and I_Y, sum together at a high impedance node which is characterized by an equivalent resistance and capacitance connected to an "ac common." A unity voltage gain stage follows the high impedance node to provide buffering from loads. Relative to either input, the open loop gain, A_{OL}, is set by the transconductance, G_M, working into the resistance, R_P; $A_{OL} = G_M \times R_P$. The unity gain frequency $\omega_{0\ dB}$ for the open loop gain is established by the transconductance, G_M, working into the capacitance, C_C; $\omega_{0\ dB} = G_M/C_C$. The open loop description of the AD830 is shown below for completeness.

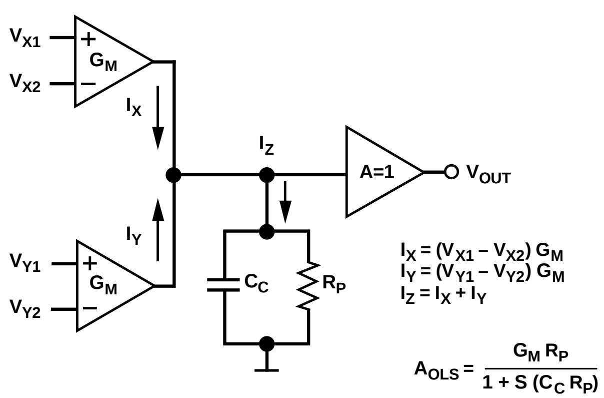


Figure 21. Topology Diagram

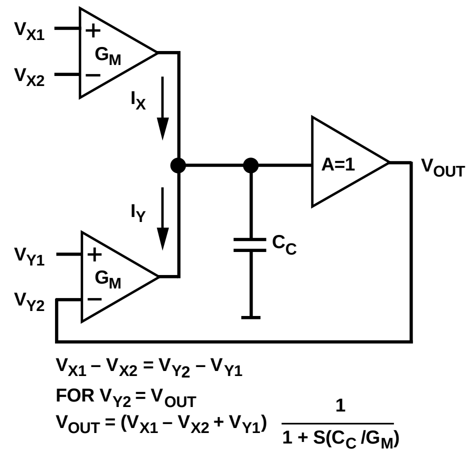


Figure 22. Closed-Loop Connection

Precise amplification is accomplished through closed-loop operation of this topology. Voltage feedback is implemented via the Y G_M stage in which where the output is connected to the –Y input for negative feedback as shown in Figure 22. An input signal is applied across the X G_M stage, either fully differentially or single-ended referred to common. It produces a current signal which is summed at the high impedance node with the output current from the Y G_M stage. Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. The error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current. Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input; $V_Y = -V_X$ or more precisely $V_{Y2}–V_{Y1} = V_{X1}–V_{X2}$. This simple relation provides the basis to easily analyze any function possible to synthesize with the AD830, including any feedback situation.

The bandwidth of the circuit is defined by the G_M and the capacitor C_C. The highly linear G_M stages give the amplifier a single pole response, excluding the output amplifier and loading effects. *It is important to note that the bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830.* In addition, the input impedance and CMRR are the same for either connections. This is very advantageous and unlike in a voltage or current feedback amplifier, where there is a distinct difference in performance between the inverting and noninverting gain. The practical importance of this cannot be overemphasized and is a key feature offered by the AD830 amplifier topology.

INTERFACING THE INPUT

Common-Mode Voltage Range

The common-mode range of the AD830 is defined by the amplitude of the differential input signal and the supply voltage. The general definition of common-mode voltage, V_{CM}, is usually applied to a symmetrical differential signal centered about a particular voltage as illustrated by the diagram in Figure 23. This is the meaning implied here for common-mode voltage. The internal circuitry establishes the maximum allowable voltage on the input or feedback pins for a given supply voltage. This constraint and the differential input voltage sets the common-mode voltage limit. Figure 24 shows a curve of the common-mode voltage range vs. differential voltage for three supply voltage settings.

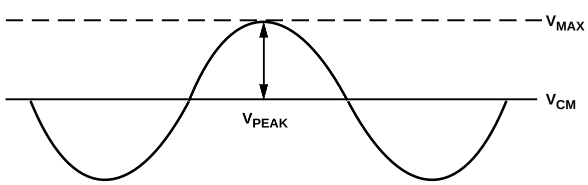


Figure 23. Common-Mode Definition

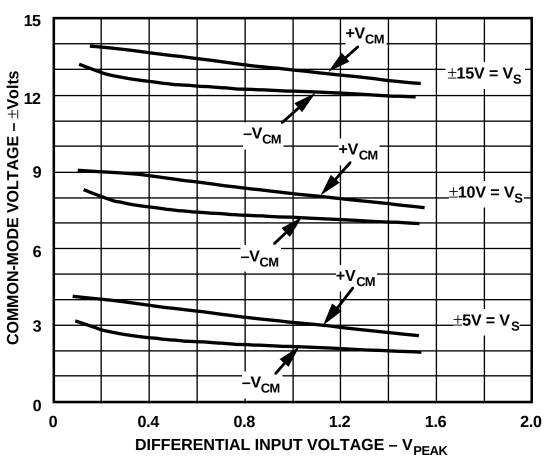


Figure 24. Input Common-Mode Voltage Range vs. Differential Input Voltage

Differential Voltage Range

The maximum applied differential voltage is limited by the clipping range of the input stages. This is nominally set at 2.4 volts magnitude and depicted in the crossplot (X-Y) photo of Figure 25. The useful linear range of the input stages is set at 2 volts, but is actually a function of the distortion required for a particular application. The distortion increases for larger differential input voltages. A plot of relative distortion versus input differential voltage is shown in Figures 8 and 11 in the Typical Characteristics section. The distortion characteristics could impose a secondary limit to the differential input voltage for high accuracy applications.

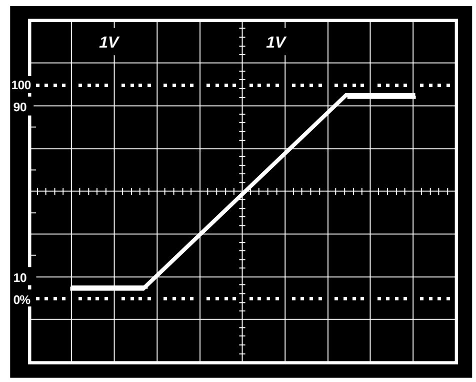


Figure 25. Clipping Behavior

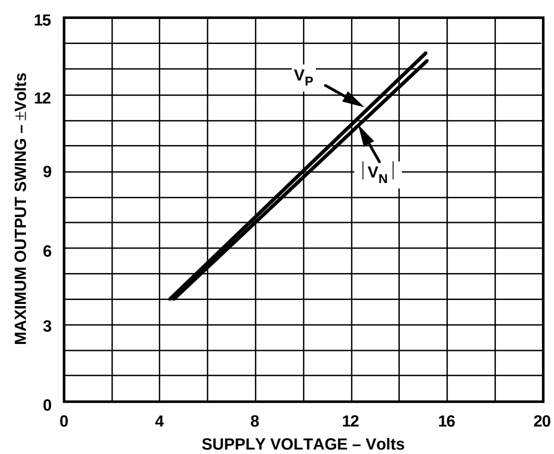


Figure 26. Maximum Output Swing vs. Supply

Choice of Polarity

The sign of the gain is easily selected by choosing the polarity of the connections to the + and – inputs of the X G_M stage. Swapping between inverting and noninverting gain is possible simply by reversing the input connections. The response of the amplifier is identical in either connection, except for the sign change. The bandwidth, high impedance, transient behavior, etc., of the AD830, is symmetrical for both polarities of gain. This is very advantageous and unlike an op amp.

Input Impedance

The relatively high input impedance of the AD830, for a differential receiver amplifier, permits connections to modest impedance sources without much loading or loss of common-mode rejection. The nominal input resistance is 300 kΩ. The real limit to the upper value of the source resistance is in its effect on common-mode rejection and bandwidth. If the source resistance is in only one input, then the low frequency common-mode rejection will be lowered to ≈ R_{IN}/R_S. The source resistance/input capacitance pole $\left(f = \frac{1}{2\pi} \times R_S \times C_{IN}\right)$ limits the bandwidth. Furthermore, the high frequency common-mode rejection will be additionally lowered by the difference in the frequency response caused by the $R_S \times C_{IN}$ pole. Therefore, to maintain good low and high frequency common-mode rejection, it is recommended that the source resistances of the + and – inputs be matched and of modest value (≤10 kΩ).

Handling Bias Currents

The bias currents are typically 4 µA flowing into each pin of the G_M stages of the AD830. Since all applications possess some finite source resistance, the bias current through this resistor will create a voltage drop ($I_{BIAS} \times R_S$). The relatively high input impedance of the AD830 permits modest values of R_S, typically ≤10 kΩ. If the source resistance is in only one terminal, then an objectional offset voltage may result (e.g., 4 µA × 5 kΩ = 20 mV). Placement of an equal value resistor in series with the other input will cancel the offset to first order. However, due to mismatches in the resistances, a residual offset will remain and likely be greater than bias current (offset current) mismatches.

Applying Feedback

The AD830 is intended for use with gain from 1 to 100. Gains greater than one are simply set by a pair of resistors connected as shown in the difference amplifier (Figure 35) with gain >1. The value of the bottom resistor R_2, should be kept less than 1 kΩ to insure that the pole formed by C_{IN} and the parallel connection of R_1 and R_2 is sufficiently high in frequency so that it does not introduce excessive phase shift around the loop and destabilizes the amplifier. A compensating resistor, equal to the parallel combination of R_1 and R_2, should be placed in series with the other Y G_M stage input to preserve the high frequency common-mode rejection and to lower the offset voltage induced by the input bias current.

Output Common Mode

The output swing of the AD830 is defined by the differential input voltage, the gain and the output common. Depending on the anticipated signal span, the output common (or ground) may be set anywhere between the allowable peak output voltage in a manner similar to that described for input voltage common mode. A plot of the peak output voltage versus supply is shown in Figure 26. A prediction of the common-mode range versus the peak output differential voltage can be easily derived from the maximum output swing as $V_{OCM} = V_{MAX} – V_{PEAK}$.

Output Current

The absolute peak output current is set by the short circuit current limiting, typically greater that 60 mA. The maximum drive capability is rated at 50 mA, but without a guarantee of distortion performance. Best distortion performance is obtained by keeping the output current ≤20 mA. Attempting to drive large voltages into low valued resistances (e.g., 10 V into 150 Ω) will cause an apparent lowering of the limit for output signal swing, but is just the current limiting behavior.

Driving Cap Loads

The AD830 is capable of driving modest sized capacitive loads while maintaining its rated performance. Several curves of bandwidth versus capacitive load are given in Figures 15 and 18. The AD830 was designed primarily as a low distortion video speed amplifier, but with a tradeoff, giving up very large capacitive load driving capability. If very large capacitive loads must be driven, then the network shown in Figure 27 should be used to insure stable operation. If the loss of gain caused by the resistor R_S in series with the load is objectionable, then the optional feedback network shown may be added to restore the lost gain.

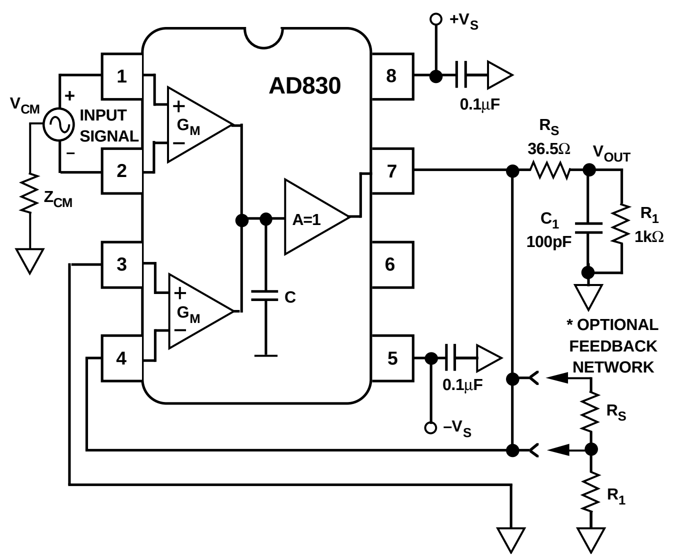


Figure 27. Circuit for Driving Large Capacitive Loads

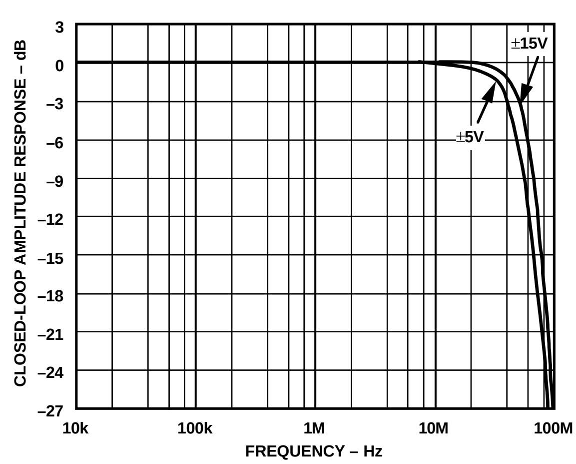
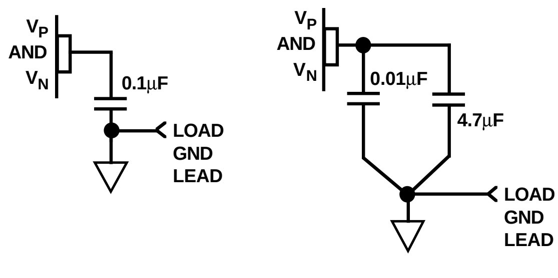


Figure 28. Closed-Loop Response vs. Frequency with 100 pF Load and Series Resistor Compensation

SUPPLIES, BYPASSING AND GROUNDING (FIGURE 29)

The AD830 is capable of operating over a wide range of supply voltages, both single and dual supplies. The coupling may be dc or ac provided the input and output voltages stay within the specified common-mode voltage limits. For dual supplies, the device works from ±4 V to ±16.5 V. Single supply operation is possible over +8 V to +33 V. It is also possible to operate the part with split supply voltages (e.g., +24 V, –5 V) for special applications such as level shifting. The primary constraint is that the total potential between the two supplies does not exceed 33 V.

Inclusion of power supply bypassing capacitors is necessary to achieve stable behavior and the specified performance. It is especially important when driving low resistance loads. At a minimum, connect a 0.1 µF ceramic capacitor at the supply lead of the AD830 package. In addition, for the best by passing, we recommend connecting a 0.01 µF ceramic capacitor and 4.7 µF tantalum capacitor to the supply lead going to the AD830.



(a) (b)

Figure 29. Supply Decoupling Options

The AD830 is designed by its functionality to be capable of rejecting noise and dissimilar potentials in the ground lines. Therefore, proper care is necessary to realize the benefits of the differential amplification of the part. Separation of the input and output grounds is crucial in rejection of the common mode noise at the inputs and eliminating any ground drops on the input signal line. For example, connecting the ground of a coaxial cable to the AD830 output common (board ground) could degrade the CMR and also introduce power-down loading on cable grounds. However, it is also necessary as in any electronic system, to provide a return path for bias currents back to their original power supply. This is accomplished by providing a connection between the differing grounds through a modest impedance labeled Z_{CM} (e.g., 100 Ω).

Single Supply Operation

The AD830 is capable of operating in single power supply applications down to a voltage of +8 V, with the generalized connection shown in Figure 30. There is a constraint on the common-mode voltage at the input and output which establishes the range for these voltages. Direct coupling may be used for input and output voltages which lie in these ranges. Any gain network applied needs to be referred to the output common connection or have an appropriate offset voltage. In situations where the signal lies at a common voltage outside the common mode range of the AD830 direct coupling will not work, so ac coupling should be used. A tested application included later in this data sheet (Figure 42), shows how to easily accomplish coupling to the AD830. For single supply operation where direct coupling is desired the input and output common-mode curves (Figures 31 and 32) should be used.

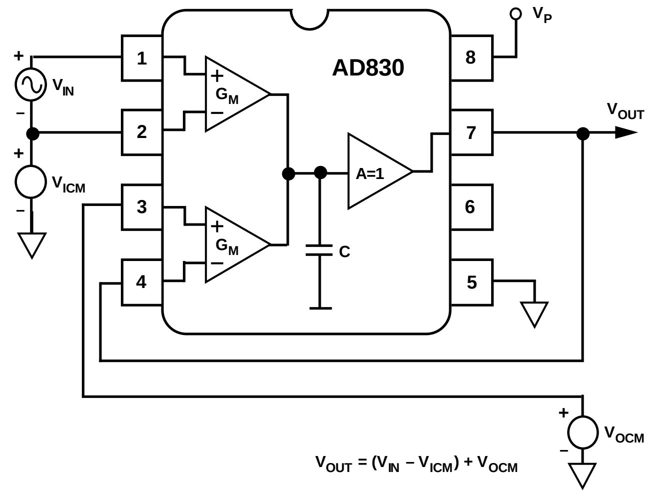


Figure 30. General Single Supply Connection

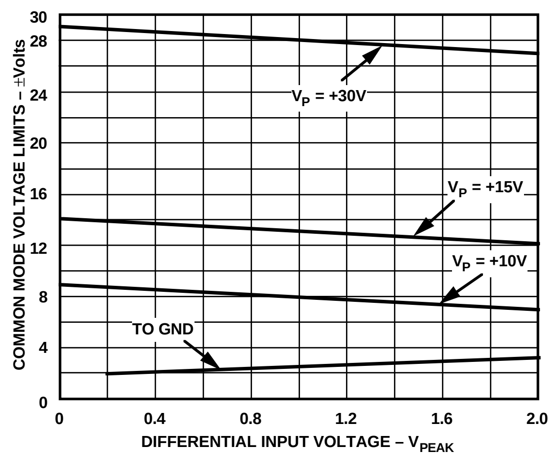


Figure 31. Input Common-Mode Range for Single Supply

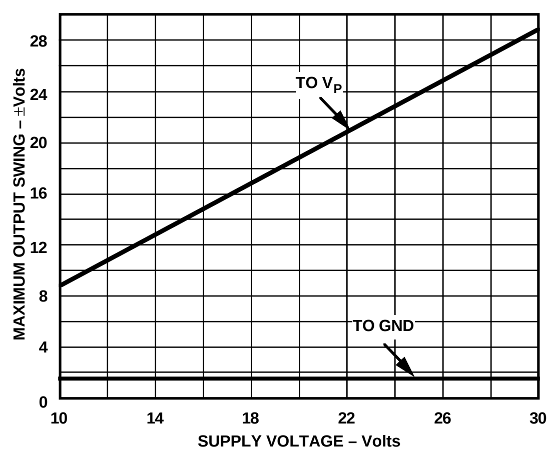


Figure 32. Output Swing Limit for Single Supply

Differential Line Receiver

The AD830 was specifically designed to perform as a differential line receiver. The circuit in Figure 33 shows how simple it is to configure the AD830 for this function. The signal from system "A" is received differentially relative to A's common, and that voltage is exactly reproduced relative to the common in system B. The common-mode rejection versus frequency, shown in Figure 1, is excellent, typically 100 dB at low frequencies. The high input impedance permits the AD830 to operate as a bridging amplifier across low impedance terminations with negligible loading. The differential gain and phase specifications are very good as shown in Figure 7 for 500 Ω and Figure 10 for 150 Ω. The input and output common should be separated to achieve the full CMR performance of the AD830 as a differential amplifier. However, a common return path is necessary between systems A and B.

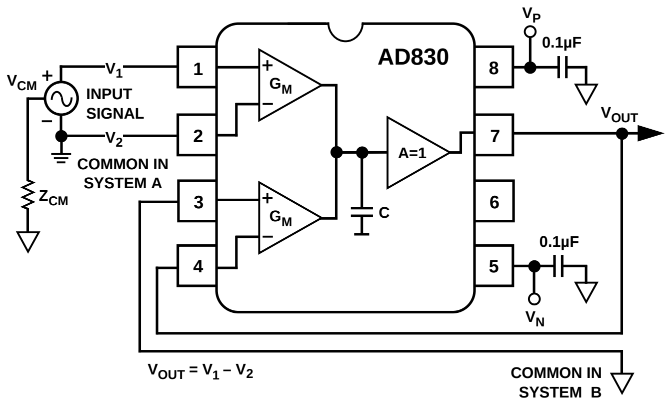


Figure 33. Differential Line Receiver

Wide Range Level Shifter

The wide common-mode range and accuracy of the AD830 allows easy level shifting of differential signals referred to an input common-mode voltage to any new voltage defined at the output. The inputs may be referenced to levels as high as 10 V at the inputs with a ±2 V swing about 10 V. In the circuit of Figure 34, the output voltage, V_{OUT}, is defined by the simple equation shown below. The excellent linearity and low distortion are preserved over the full input and output common-mode range. The voltage sources need not be of low impedance, since the high input resistance and modest input bias current of the AD830 V-to-I converters permit the use of resistive voltage dividers as reference voltages.

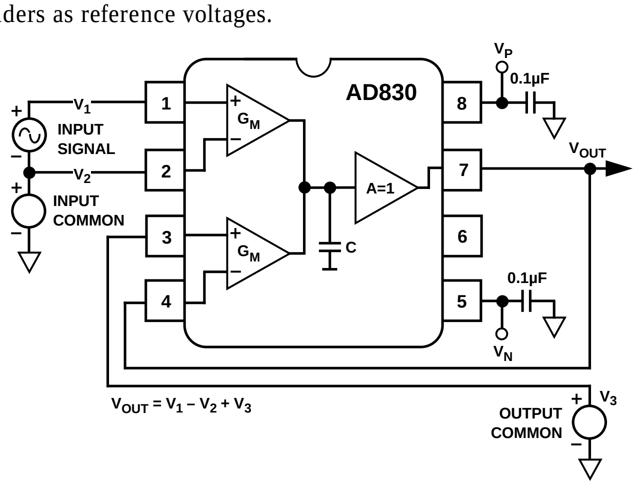


Figure 34. Differential Amplification with Level Shifting

Difference Amplifier with Gain > 1

The AD830 can provide instrumentation amplifier style differential amplification at gains greater than 1. The input signal is connected differentially and the gain is set via feedback resistors as shown in Figure 35. The gain, $G = (R_2 + R_1)/R_2$. The AD830 can provide either inverting or noninverting differential amplification. The polarity of the gain is established by the polarity of the connection at the input. Feedback resistors R_2 should generally be $R_2 \le 1$ kΩ to maintain closed-loop stability and also keep bias current induced offsets low. Highest CMRR and lowest dc offsets are preserved by including a compensating resistor in series with Pin 3. The gain may be as high as 100.

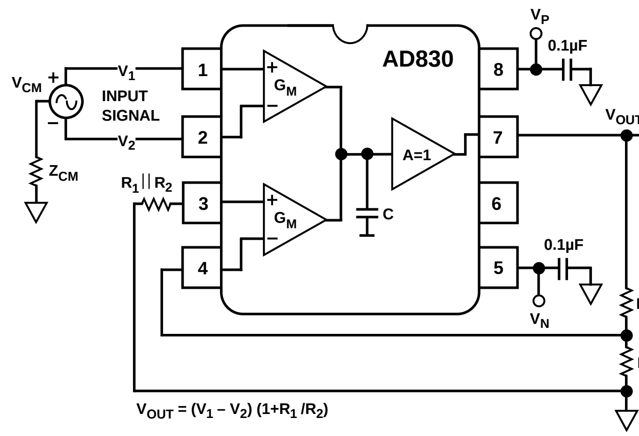


Figure 35. Gain of G Differential Amplifier, G > 1

Offsetting the Output with Gain

Some applications, such as A/D drivers, require that the signal be amplified and also offset, typically to accommodate the input range of the device. The AD830 can offset the output signal very simply through Pin 3 even with gain > 1. The voltage applied to Pin 3 must be attenuated by an appropriate factor so that $V_3 \times G$ = desired offset. In Figure 36, a resistive divider from a voltage reference is used to produce the attenuated offset voltage.

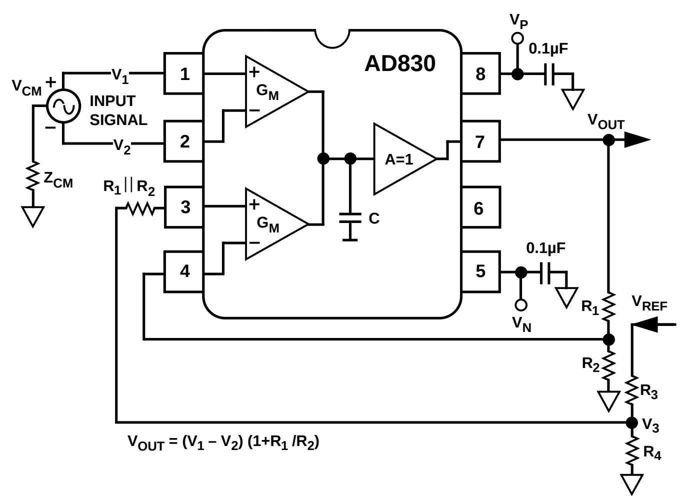


Figure 36. Offsetting the Output with Differential Gain > 1

Loop Through or Line Bridging Amplifier (Figure 37)

The AD830 is ideally suited for use as a video line bridging amplifier. The video signal is tapped from the conductor of the cable relative to its shield. The high input impedance of the AD830 provides negligible loading on the cable. More significantly, the benign loading is maintained while the AD830 is powered-down. Coupled with its good video load driving performance, the AD830 is well suited to video cable monitoring applications.

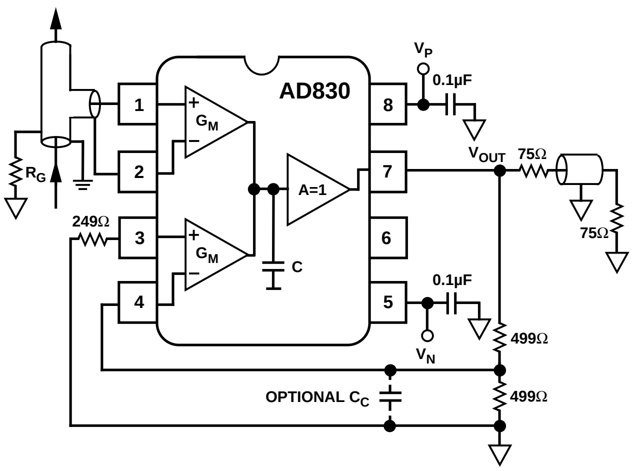


Figure 37. Cable Tap Amplifier

Resistorless Summing

Direct, two input, resistorless summing is easily realized from the general unity gain mode. By grounding V_{X2} and applying the two inputs to V_{X1} and V_{Y1}, the output is the exact sum of the applied voltages V_1 and V_3, relative to common; $V_{OUT} = V_1 + V_3$. A diagram of this simple, but potent application is shown below in Figure 38. The AD830 summing circuit possesses several virtues not present in the classic op amp based summing circuits. It has high impedance inputs, no resistors, very precise summing, high reverse isolation and noninverting gain. Achieving this function and performance with op amps requires significantly more components.

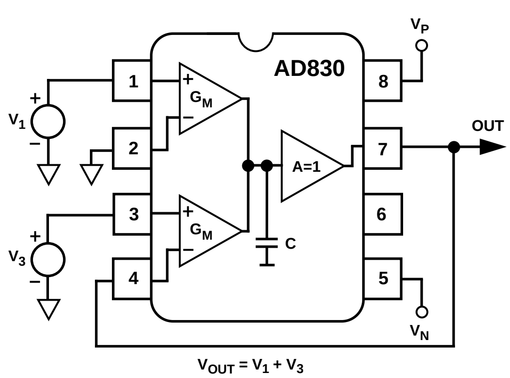


Figure 38. Resistorless Summing Amplifier

2× Gain Bandwidth Line Driver

A gain of two, without the use of resistors, is possible with the AD830. This is accomplished by grounding V_{X2}, tying the two inputs V_{X1} and V_{Y1} together and applying the input, V_{IN}, to this wired connection. The output is exactly twice the applied voltage, V_{IN}; $V_{OUT} = 2 \times V_{IN}$. Figure 39 below shows the connections for this highly useful application. The most notable characteristic of this alternative gain of two is that there is no loss of bandwidth as in a voltage feedback op amp based gain of +2 where the bandwidth is halved, therefore, the gain bandwidth is doubled. Also, this circuit is accurate without the need for any precise valued resistors, as in the op amp equivalents, and it possess excellent differential gain and phase performance as shown in Figures 40 and 41.

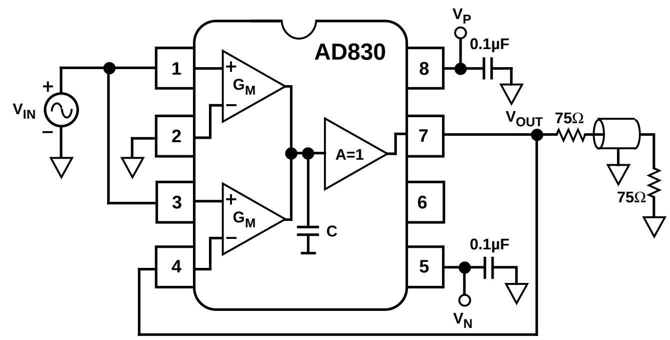


Figure 39. Full Bandwidth Line Driver (G = +2)

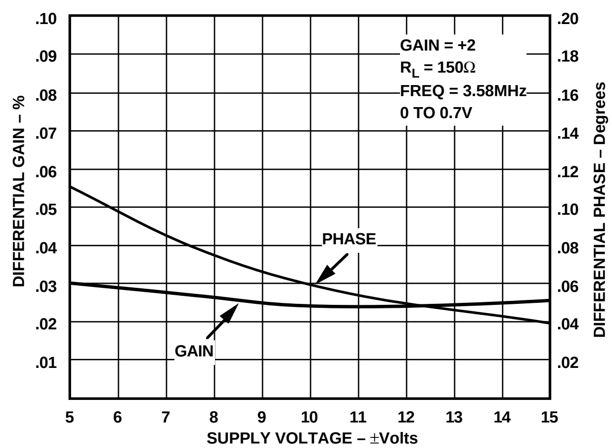


Figure 40. Differential Gain and Phase for the Circuit of Figure 39

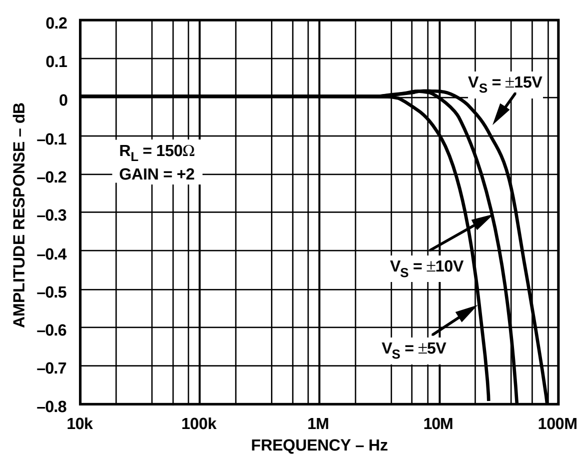


Figure 41. 0.1 dB Gain Flatness for the Circuit of Figure 39

AC COUPLED LINE RECEIVER

The AD830 is configurable as an ac coupled differential amplifier on a single or bipolar supply voltages. All that is needed is inclusion of a few noncritical passive components as illustrated below in Figure 42. A simple resistive network at the X G_M input establishes a common-mode bias. Here, the common mode is centered at 6 volts, but in principle can be any voltage within the common-mode limits of the AD830. The 10 kΩ resistors to each input bias the X G_M stage with sufficiently high impedance to keep the input coupling corner frequency low, but not too large so that residual bias current induced offset voltage becomes troublesome. For dual supply operation, the 10 kΩ resistors may go directly to ground. The output common is conveniently set by a Zener diode for a low impedance reference to preserve the high frequency CMR. However, a simple resistive divider will work fine and good high frequency CMR can be maintained by placing a compensating resistor in series with the +Y input. The excellent CMRR response of the circuit is shown in Figure 43. A plot of the 0.1 dB flatness from 10 Hz is also shown. With the use of 10 µF capacitors, the CMR is >90 dB down to a few tens of hertz. This level of performance is almost impossible to achieve with discrete solutions.

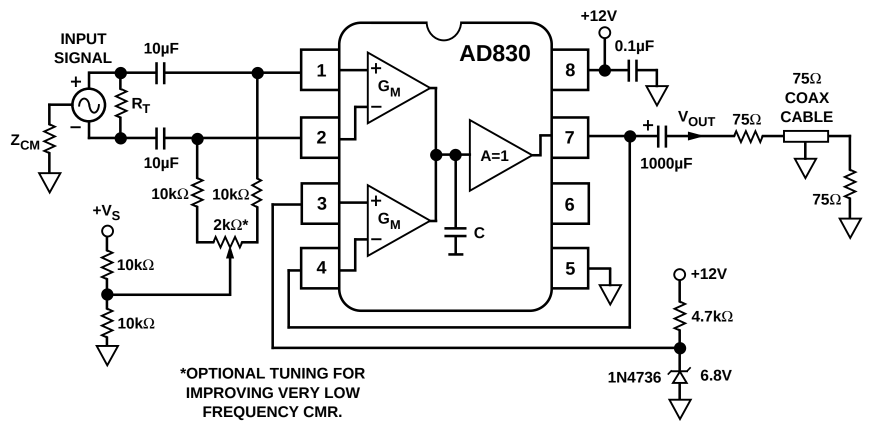


Figure 42. AC Coupled Line Receiver

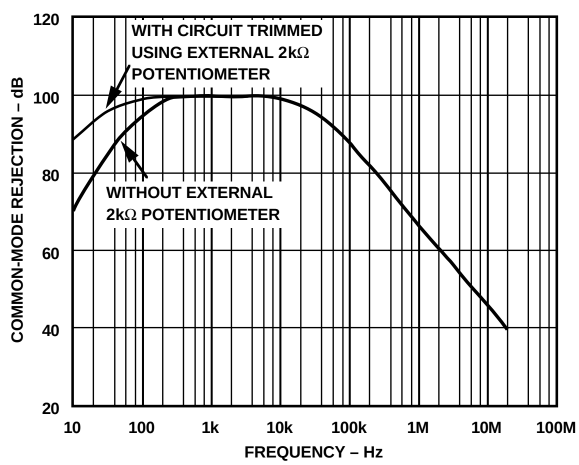


Figure 43. Common-Mode Rejection vs. Frequency for Line Receiver

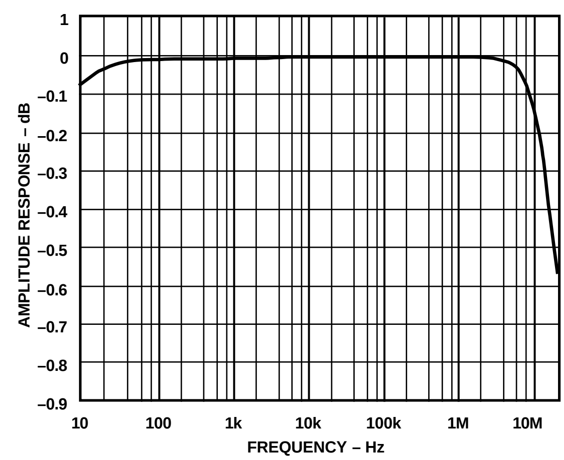
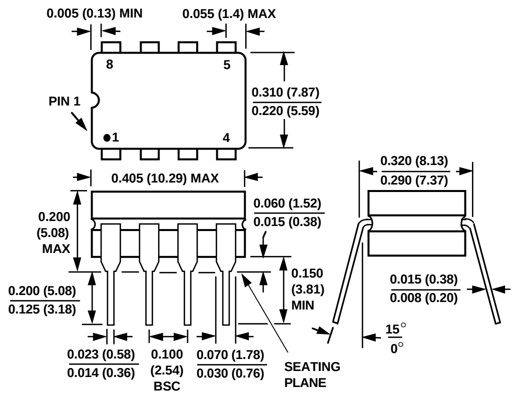


Figure 44. Amplitude Response vs. Frequency for Line Receiver

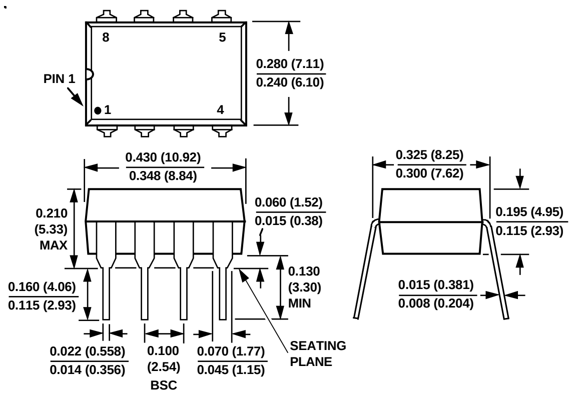
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

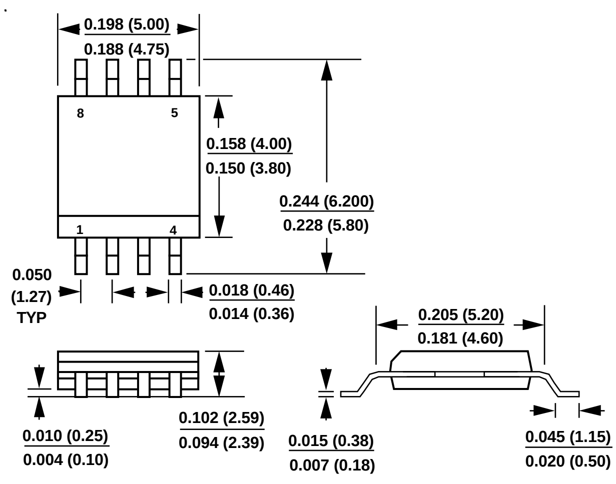
Cerdip (Q) Package



Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



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